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Power Quality Improvement and PV Power Injection by DSTATCOM with Variable DC Link Voltage Control from RSC-MLC

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***Abstract*—The study proposes a method to optimize dc-link voltage of Distribution Static Compensator (DSTATCOM) based on load compensation requirement using Reduced Switch Count Multi-Level Converter (RSC-MLC) integrated with Photo-Voltaic (PV) system. The proposed method is capable of compensating reactive power, unbalance and harmonics demanded by three-phase unbalanced and non-linear loads connected to the distribution side, leading to improvement of power quality. It is also capable of providing real power support to the load and thus prevents source from getting over loaded whenever required. During off-peak loads, the dc-link voltage can be brought down to a lower value, which will reduce the voltage-stress across switches of inverter and minimizes the switching losses. The variation of dc-link voltage is provided using RSC-MLC which requires dc voltage supply. This method utilizes renewable resources of energy such as solar cells as the dc voltage source. The output voltage of PV panel is boosted to a higher value using High Gain Boost Converter (HGBC) and given to RSC-MLC. The maximum power point tracking (MPPT) of PV panels is achieved by using Perturb and Observe (P & O) algorithm. The results have been verified through simulation and experimental studies.**

***Index Terms*—DC-link voltage, DSTATCOM, Power Quality, PV system, Reduced Switch Count Multi Level Converter (RSC-MLC), Switching Losses.**

I. Introduction

The proliferation of non-linear, inductive and unbalanced loads in the distribution system has led to several power quality issues [1]. It is due to rapid rise in the use of sensitive equipment in industrial, commercial, domestic and traction applications such as switched mode power supplies, computers, refrigerators, televisions etc. The utilization side demands controlled supply of power which involves the use of power electronic converters. The generators produce a sinusoidal voltage but the currents drawn by such loads are distorted and unbalanced. This affects the feeder voltage and leads to malfunctioning of other loads connected to the same feeder. Several custom power devices (CPDs) have been used to overcome these issues [2], [3]. Out of these CPDs, Distribution Static Compensators (DSTATCOMs) are extensively used for mitigating the current-based power quality problems which include poor power factor, unbalanced currents and increased neutral current. Several DSTATCOM topologies and their design have been covered in existing literature based on the requirement. Some conventional methods are 4-leg DSTATCOM and split-capacitor DSTATCOM [4], [5]. The 4-leg DSTATCOM topology uses one extra leg to provide the path for neutral current. This involves the use of extra switches leading to more switching losses. Split capacitor DSTATCOM suffers from capacitive voltage unbalance problem due to unequal charging of two capacitors at dc-link. In this paper, 3-leg Voltage Source Inverter (VSI) topology with neutral capacitor has been used, which overcomes these issues [6]. It uses only one capacitor at the dc-link, so there is no capacitor voltage unbalance. Also, there is no need to introduce an extra leg with two more switches because the neutral current compensation is taken care by the small rated neutral capacitor. However, in most of the mentioned topologies, the dc-link voltage is kept constant based on rated load conditions [7]. This leads to unnecessary switching losses at reduced loads. The dc-link voltage can be reduced at reduced loads for minimization of switching losses associated with Voltage Source Inverter (VSI) without affecting compensation. In [8], adaptive dc-link voltage variation has been proposed using PI controller. However, it suffers from slow transient response due to the behavior of PI controller and leads to rippled dc-link voltage which makes it unreliable for fast changing loads.

In the proposed method, the dc-link voltage regulation is achieved using Reduced Switch Count Multi Level Converter (RSC-MLC). The gate pulses of inverter switches are controlled using Hysteresis Controller which is faster and simpler [9]. The gate pulses are derived using Instantaneous Symmetrical Component Theory (ISCT) to get the reference harmonic currents based on load demand [10]. These harmonic currents are used to find the required reference dc-link voltage. The RSC-MLC is operated using Pulse Width Modulation (PWM) technique to obtain the desired level of dc-link voltage. The specialty of this RSC-MLC topology is reduced voltage stress at any operating condition across switches, which leads to reduction in switching losses.

Due to growing consumption of conventional sources of energy, there is a huge need to employ non-conventional resources in as many applications possible because they are freely available as well as non-polluting [11]. The solar energy is viewed as one of the popular and potential energy source for meeting the demands. The solar energy is converted into electrical energy by using Photo Voltaic (PV) cells. Several analysis upon the stability and performance of the PV integrated systems for various applications have been performed [12], [13], [14]. In the proposed method, the PV panels are used to charge the batteries of RSC-MLC. The Maximum

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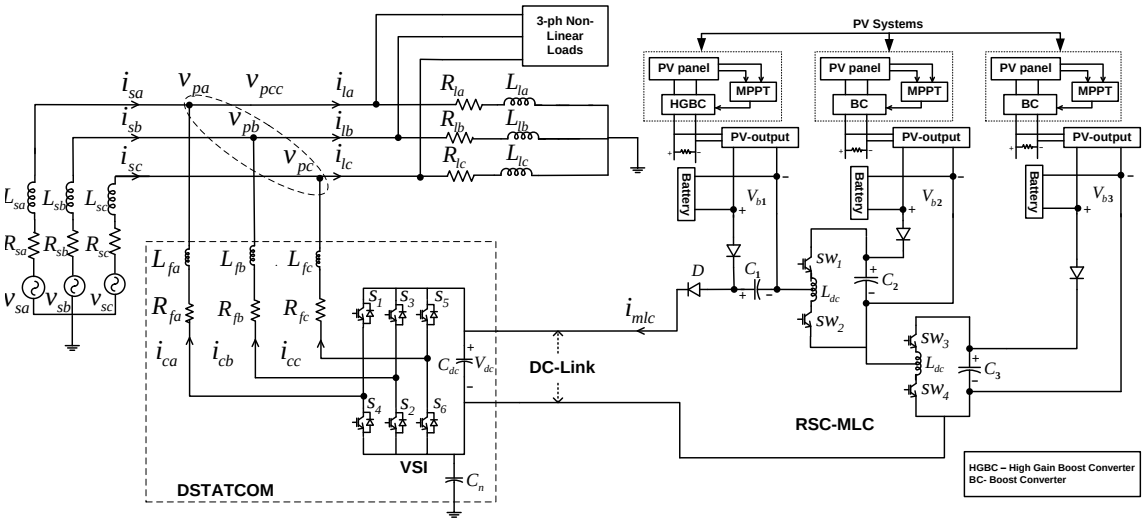

Fig. 1: RSC-MLC controlled DSTATCOM for PQ improvement and real power injection from PV in distribution system.

Power Point Tracking (MPPT) is achieved using Perturb & Observe (P & O) algorithm and the output voltage of PV panel is stepped up using High Gain Boost Converter (HGBC) [15].

During day time, PV panels produce maximum real power. Therefore, the batteries can be charged and real power support can also be provided. At night, PV panels cannot deliver real power due to insufficient irradiation. In this case, the batteries will support the dc-link voltage for reactive power and harmonic compensation. The real power can be shared intelligently based upon the availability of irradiation and demand. The complete details of dc-link voltage variation using proposed RSC-MLC for achieving power quality improvement and injection of real power is discussed below extensively.

II. Proposed Operation of DSTATCOM using RSC-MLC Integrated with PV-panels.

The schematic diagram of DSTATCOM for power quality improvement and PV power injection with RSC-MLC on dc-side of VSI is shown in Fig. 1. In most of the existing topologies of VSI, the dc-link voltage is maintained constant ($i.e.$, twice the peak of V_{pcc}) for all load conditions [7]. But, in reality the dc-link voltage required is low when system is operated at off-peak load conditions. Therefore, constant rated dc-link voltage leads to unwanted switching losses during reduced load conditions. The dc-link voltage can be reduced at off-peak loads without compromising the compensation. This reduces the voltage stress across switches of VSI and minimizes the switching losses at reduced loads.

In the proposed method, RSC-MLC is used for regulating the dc-link voltage of DSTATCOM. At reduced loads, it reduces the dc-link voltage which leads to minimization of switching losses. The operation of RSC-MLC and selection of dc-link voltage based on various load requirements is explained here in detail. The dc-voltage sources used for RSC-MLC are PV-Panels which is a source of real power. Hence, the real power sharing can also be achieved based on availability of sunlight and the load demand. The reference dc-link voltage for the proposed method is estimated as shown

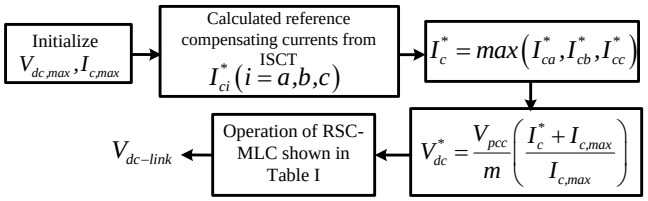

Fig. 2: Flow-chart for reference dc-link voltage calculation.

in Fig. 2 [8]. In Fig. 2, $I_{c,max}$ is maximum compensating current compensated by DSTATCOM for a given rated load condition. The reference rms compensating currents (I_{ci}^*) are derived from the instantaneous reference compensating currents obtained using ISCT [16], as given in (1).

$$i_{ck}^* = i_{lk} - \left(\frac{v_{sk}}{\sum_{j=a,b,c} v_{sj}^2}\right) P_l \tag{1}$$

where, k = a, b and c phases. v_{sk} is supply phase voltages, i_{lk} is load currents, i_{ck} represents the reference compensating currents and P_l is the average real power demanded by the load. However, the final dc-link voltage (V_{dc}) is selected based on the ranges of reference dc voltage (V_{dc}^*) using RSC-MLC. The maximum dc-link voltage ($V_{dc,max}$) in the proposed method is considered as twice of 1.6 times peak of PCC voltage [6]. The dc-link voltage and corresponding switches operated in RSC-MLC are shown in Table. I.

TABLE I: DC-link voltages corresponding to switching devices of RSC-MLC

Ranges of V_{dc}^*	Operating switches in RSC-MLC	DC-link voltage
$< V_{dc,min}$	sw_2, sw_4	V_{b1}
$V_{dc,min} - V_1$	$sw_1(d_1)$, sw_4	V_{b1}+V_{b2}*d_1
$V_1 - V_2$	$sw_1(d_2)$, sw_4	V_{b1}+V_{b2}*d_2
$V_2 - V_3$	sw_1, sw_4	V_{b1}+V_{b2}
$V_3 - V_4$	sw_1, $sw_3(d_1)$	V_{b1}+V_{b2}+V_{b3}*d_1
$V_4 - V_5$	sw_1, $sw_3(d_2)$	V_{b1}+V_{b2}+V_{b3}*d_2
$V_5 - V_{dc,max}$	sw_1, sw_3	V_{b1}+V_{b2}+V_{b3}

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The dc-link voltage levels is divided equally in steps from $V_{dc,min}$ to $V_{dc,max}$. The voltage range from $V_{dc,min}$ to $V_{dc,max}$ is divided such that with each subsequent operation of switch, the following increment in voltage step (ΔV_{dc}) is obtained.

$$\Delta V_{dc} = \frac{V_{dc,max} - V_{dc,min}}{6} \tag{2}$$

Hence the voltage varies in steps such as $V_{dc,min}$, ($V_{dc,min} + \Delta V_{dc}$), ($V_{dc,min} + 2\Delta V_{dc}$), ..., $V_{dc,max}$, based on the calculated V_{dc}^{*} value corresponding to load. The RSC-MLC is basically a type of buck-converter which steps down the input dc voltage by the factor of duty-cycle. To get the desired voltages, the switches of RSC-MLC are operated with certain duty cycles. Here, the duty cycle $d_1 = 1/3$ and $d_2 = 2/3$ are selected to obtain the equal voltage division between $V_{dc,min}$ to $V_{dc,max}$ by getting the desired increment ΔV_{dc} in the dc-link voltage. Here, $V_{dc,min}$ is same as the voltage across battery (V_{b1}) and $V_{dc,max} = V_{b1} + V_{b2} + V_{b3}$. By selection of such duty cycles, the value of dc-link voltage are shown in Table I. For example : (a) $V_{dc,min} = V_{b1}$ obtained by switching ON sw_2 and sw_4 permanently, (b) $V_{dc,min} + \Delta V_{dc} = V_{b1} + V_{b2} * d_1$ and $V_{dc,min} + 2\Delta V_{dc} = V_{b1} + V_{b2} * d_2$ are obtained by keeping sw_4 ON and operating sw_1 with duty cycles d_1 and d_2, respectively. In the similar way, to get $V_{dc,max}$, sw_1 and sw_3 are switched ON permanently.

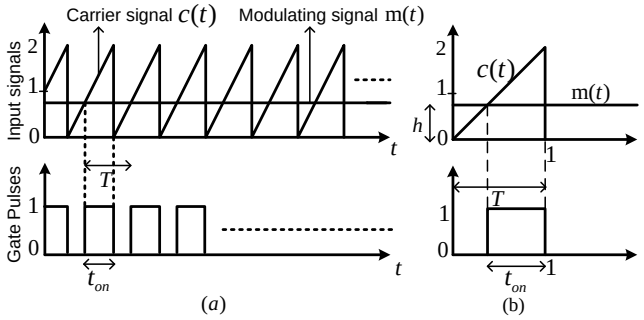

Fig. 3: Generation of gate pulses from carrier signal and modulating signal.

The duty cycles d_1 and d_2 are obtained and gate pulses are generated for the switches sw_1 to sw_4 using sawtooth-step PWM technique as shown in Fig. 3(a). The gate pulses are generated by comparing carrier signal ($c(t)$) and modulating signal ($m(t)$). If $c(t) > m(t)$, gate pulse is logic one ($i.e.$, ON period (t_{on}), otherwise logic zero ($i.e.$, OFF period). By varying the magnitude of modulating signal, the t_{on} period can be varied, which is explained below. From similarity of the triangles of the figure shown in Fig. 3(b), the following relation can be written,

$$\frac{h}{T - t_{on}} = \frac{2}{T} \tag{3}$$

where, T is total time period of pulse, h be the magnitude of modulating signal. The expression of duty cycle d for operation of switches can be given as $d = t_{on}/T$.

By varying the frequency of carrier signal, both the t_{on} and T changes, such that the duty cycle remains same. Therefore, for simplicity in calculation, the time-period T is scaled down to 1 ($i.e.$ $T = 1$). For duty cycle $d_1 = 1/3$, $t_{on} = 1/3$, the calculated value from (3) is $h = 4/3$. Similarly, for duty cycle $d_2 = 2/3$, $t_{on} = 2/3$, $h = 2/3$ is obtained. Therefore the modulating signals of magnitude $h = 4/3$ and $h = 2/3$ is used to get $d_1 = 1/3$ and $d_2 = 2/3$ respectively. By operating the switches of RSC-MLC with these duty cycles, the output voltage levels can be varied in equal steps with improved flexibility. Hence, at reduced loads, the switching losses in VSI are minimized because of reduced dc-link voltage. Here, seven dc voltage levels have been achieved using the RSC-MLC shown given in Fig. I.

A. Designing of RSC-MLC Parameters

Design of dc-link inductor (L_{dc}): The proper design of dc-link inductor is important in order to eliminate the current ripples and allows to achieve the voltage variations in smooth manner. The RSC-MLC is basically working as dc-dc buck converter with modified features.

Let, f_{sw} =switching frequency, $\Delta I_{L,max}$ =maximum current ripple through inductor, L_{dc} =dc-link inductance. Then, from the basic equations of buck converter, following equation is obtained [17].

$$\Delta I_{L,max} = \frac{V_{b2} \ \ (or) \ \ V_{b3}}{4 L_{dc} f_{sw}} \tag{4}$$

The inductor, L_{dc} is designed based on $\Delta I_{L,max}$. In this paper, $V_{b2} = 200$ V, $f_{sw} = 10$ kHz, $\Delta I_{L,max} = 0.1$ A. After substituting all these values, the value of $L_{dc} = 50$ mH.

Design of capacitors: The dc-link capacitor plays a major role in eliminating the voltage ripples and maintaining the output voltage of RSC-MLC. Since, the RSC-MLC is using dc-voltage sources in the form of PV panels, the ripple in the voltage is already very less. Hence the rating of the capacitor is very less. Let, $\Delta V_{o,max}$ be the maximum voltage ripple across dc-link capacitor and C_{dc} is dc-link capacitance. Then from the buck converter basic equations [17],

$$\Delta V_{o,max} = \frac{V_{dc}}{32 L_{dc} C_{dc} f_{sw}^2} \tag{5}$$

For better performance, the allowable ripple voltage is considered as 3% of V_{dc}. By substituting the values in (5), the obtained capacitor value is, C_{dc} = 0.2 μF.

The capacitors C_1, C_2 and C_3 shown in Fig. 1 are connected in parallel to the PV panels. They help in eliminating the voltage ripples at the output of PV panel, and also used for charging the batteries connected in parallel to them. The design of these capacitors depend on the voltage rating and current through them. Their values are estimated using following expressions, q=CV_C where q is charge and V_C is rated voltage across capacitor having capacitance C. So,

$$I_C = \frac{C \Delta V_C}{\Delta t} \tag{6}$$

where I_C= current through C, ΔV_C= peak to peak ripple voltage across C, $\Delta t = 1/f_{sw}$. Substituting and rearranging the terms, following expression is obtained.

$$C = \frac{I_C}{f_{sw} \Delta V_C} \tag{7}$$

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Here, the capacitors C_1, C_2 and C_3 are connected across PV panels of rated output voltage (V_C) 700 V, 200 V and 200 V respectively. Here, ΔV_C=3% of V_C, I_C= 0.5 A as maximum allowable current through capacitors and f_{sw}=10 kHz are considered. Substituting these values, the values of capacitors, C_1=2.38 μF, C_2=8.33 μF and C_3=8.33 μF are obtained.

B. Generation of Gate Pulses for DSTATCOM.

The control algorithm of gate pulses generation for DSTATCOM is shown in Fig. 4. The reference compensating currents are derived using ISCT [16]. These reference compensating currents are compared with actual compensating currents supplied by DSTATCOM and error is given to hysteresis controller. It generates gate pulses, which will operate the DSTATCOM in such a way that it injects exactly the same compensating current required by the load.

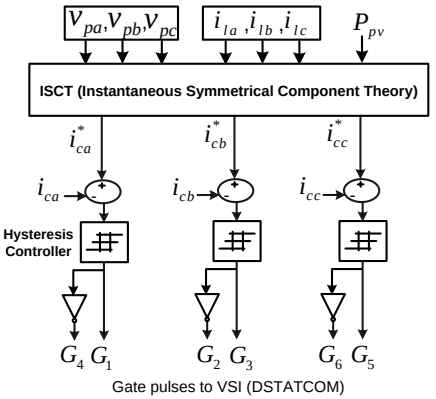

Fig. 4: Control algorithm of gate pulse generation for DSTATCOM.

Hence, the DSTATCOM is able to compensate the harmonic current and reactive power demanded by the load and also supplies the real power generated from PV system. Therefore, source current becomes free from harmonics and supplies only real power, improving the source power factor.

C. PV panels- MPPT and real power injection

Some portion of the real power demanded by the load can be compensated through PV panels integrated with DSTATCOM. The renewable sources of energy have always been a prospective source for several applications due to its free availability and environment-friendly nature. The present paper utilizes solar energy captured using PV panels as dc voltage sources to RSC-MLC. PV panel voltage is boosted to desired voltage value using a BC (Boost Converter) or HGBC (High Gain Boost Converter) [15]. The P and O algorithm is used for extracting the maximum power from PV panels [18].

The RSC-MLC shown in Fig. 1 is having capacitors C_1, C_2 and C_3 for eliminating the voltage ripples at the output of PV panels. The capacitor C_1 is charged to 700 V which is the minimum dc-link voltage requirement and C_2, C_3 are charged to a voltage of 200 V each. For getting 700 V, a HGBC is used across the PV panel. To get 200 V, normal BC is sufficient. The obtained dc voltage is used to charge the batteries through charge controller. The batteries are connected across the corresponding capacitors to maintain the dc voltage. The batteries are designed based on the requirement of voltage and power to be supplied [19]. In the proposed method, the voltage and power rating of the battery are considered as 200 V and 2000 W, respectively.

The solar energy captured by PV panels keeps changing with time and environmental conditions. Based on availability of irradiation, the combination of PV integrated with DSTATCOM can be operated in different modes. They are explained in detail along with waveforms in simulation studies.

III. Simulation Studies

The simulation parameters used in the proposed system are mentioned in Table II. The simulation is performed for seven non-linear and unbalanced loads added one after another in an interval of 0.2 s, as mentioned in Table II (Case I to Case VII, where the Case VII is considered as rated load condition).

TABLE II: Simulation Parameters

Symbol	System parameters	Values
V_s	Supply voltage	400 V (L-L), 50 Hz
R_s, L_s	Source impedance	0.2 Ω, 0.1 mH
L_f	Interfacing inductance	20 mH
C_{dc}	dc-link capacitance	0.2 μF
L_{dc}	dc-link inductance	50 mH
C_n	neutral capacitance	39 μF
C_1, C_2, C_3	Capacitances across PV panel	2.38 μF, 8.33 μF, 8.33 μF
h	Hysteresis band	$\pm$ 0.8 A
Load-1 (L1)	3-ph diode bridge load	250 Ω , 300 mH
Load-2 (L2)	3-ph diode bridge load	150 Ω , 90 mH
Load-3 (L3)	Unbalanced linear load	*a*-ph : 100 Ω , 160 mH
	(Y connected load)	*b*-ph : 120 Ω , 170 mH
		c-ph : 108 Ω , 160 mH
Load-4 (L4)	Unbalanced linear load	*a*-ph : 102 Ω , 160 mH
	(Y connected load)	*b*-ph : 120 Ω , 165 mH
		c-ph : 100 Ω , 162 mH
Load-5 (L5)	3-ph diode bridge load	80 Ω , 70 mH
Load-6 (L6)	3-ph diode bridge load	250 Ω , 90 mH
Load-7 (L7)	3-ph diode bridge load	245 Ω , 100 mH
$V_{dc,max}$	Maximum dc-link voltage	1100 V

Load changes in simulation :							
Time (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-0.8	0.8-1	1-1.2	1-1.4
Cases	I	II	III	IV	V	VI	VII
Load	L1	L1+L2	L1+..L3	L1+...L4	L1+...L5	L1+...L6	L1+...L7

A. PV-DSTATCOM modes of operation

The PV panel with RSC-MLC can be operated in different modes based on availability of irradiation. It is discussed here in detail.

Mode I: During night hours or cloudy atmosphere, the PV panels cannot generate sufficient real power to meet the load demand due to insufficient irradiation. However, the charged batteries will support to maintain the dc-link voltage by taking a small amount of real power. Therefore, reactive power compensation, harmonic mitigation and load balancing are achieved in this mode. They cannot inject any real power into the system. Since the reactive power demanded by the load is compensated fully by the DSTATCOM, the source need not supply any reactive power. Hence, the source power factor gets improved significantly (nearly unity). The reactive powers flow during compensation by DSTATCOM are shown in Fig. 5. It is observed that, the reactive power required for load is supplied by DSTATCOM.

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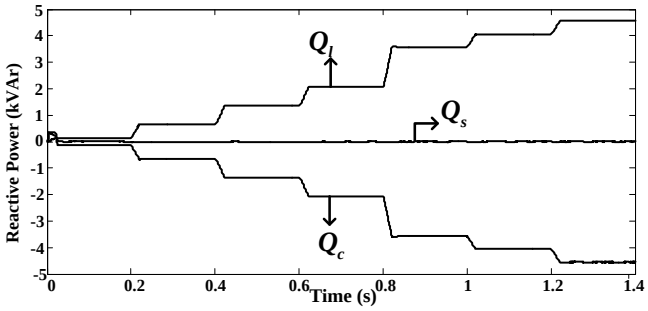

Fig. 5: Reactive powers flow in mode-1: Q_l is load reactive power, Q_s is source reactive power and Q_c is reactive power compensated by DSTATCOM.

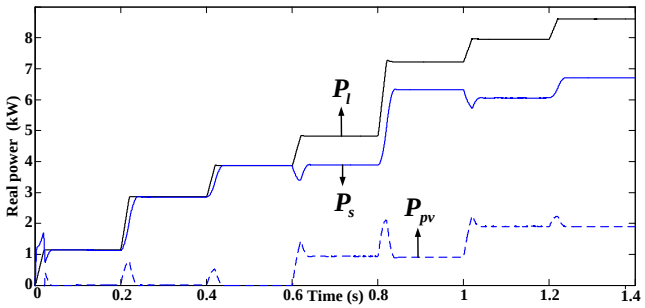

Fig. 7: Real power flow for different irradiations in mode-2: P_l is load power, P_s is source power and P_{pv} is power supplied by PV panels.

Mode II: PV panels provide maximum output power when irradiation is sufficient (day time with full sunshine). Hence, DSTATCOM can share some of the real power demanded by the load as well as work for improvement of power quality. For better understanding, this mode is explained for constant and variable irradiation with MPPT powers as shown in Fig. 6.

Constant Irradiation: Fig. 6(a) shows MPPT power for constant irradiation. This case prevails during day time, when the effective sun-rays reaching PV panels are almost constant and rated for significant time. In this case, the real power from the PV panels is maximum and nearly constant.

Variable Irradiation: Fig. 6(b) shows MPPT power for variable irradiation. This case prevails when the available sun-light is changes with time. It can be during cloudy atmosphere or transition state of the sun. In this case, the effective irradiation to the PV panel varies and hence the maximum real power output of PV panel changes.

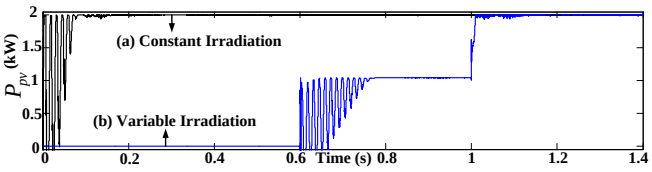

Fig. 6: MPPT power (P_{pv}) (a) constant irradiation: G=1000 W/m^2, (b) variable irradiation: G=0 W/m^2 (0 s to 0.6 s), G=500 W/m^2 (0.6 s to 1 s) and G=1000 W/m^2 (1 s to 1.4 s).

The real power sharing by PV panel and source to meet the load demand is shown in Fig. 7. Here, the PV panel is injecting no power from 0 to 0.6 s (night time), 1 kW power from 0.6 to 1 s (partial irradiation) and 2 kW power from 1 s to 1.4 s (full irradiation). It is observed that, when PV is injecting some real power (P_{pv}), the real power supplied by the source (P_s) reduces by the same amount. This real power support can prevent frequent load-shedding and over-loading of source/grid, making the distribution system more reliable and efficient.

The complete simulation waveforms to demonstrate the power quality improvement along with real power injection is shown in two figures, Fig. 8 from t=0.1 s to t=0.7 s and Fig. 9 from t=0.7 s to t=1.3 s. From these figures, the waveform i_l shows the non-linearity and unbalance present in the load current based on the cases of load addition listed in Table II. The reactive power, harmonics and unbalance demand by load are compensated by DSTATCOM. Therefore, the source current (i_s) is supplying only real power, balanced and free from harmonics. Table III gives the comparison of %Total Harmonic Distortion (% THD) of source current and source side power factor before and after compensation. It shows that %THD has reduced and power factor has improved greatly in the source side after compensation. In Fig. 8 and Fig. 9 (c) and (d), real power of 1 kW is injected from t = 0.6 s to 1 s and 2 kW from t = 1 s to 1.3 s. It is also observed that when real power is injected using PV, there is a decrease in magnitude of source current, showing the reduction in real power supplied by source. This prevents source over-loading and load-shedding.

The waveforms in Fig. 8 and Fig. 9 show the source currents for both the cases, one with only in DSTATCOM mode and another with variable real power injection through PV. When real power is injected, the demand for real power from the source decreases. It can be observed from the reduction in magnitude of i_s after real power injection. This reduction in source current prevents the overloading of source and load-shedding.

TABLE III: %THD of source current and source side power factor before and after compensation for different load conditions.

Cases	%THD before			%THD after			Power factor	
	I_{sa}	I_{sb}	I_{sc}	I_{sa}	I_{sb}	I_{sc}	Before	After
I	26.9	26.9	26.9	4.9	4.9	4.9	0.95	1
II	24.75	24.75	24.75	2.43	2.43	2.43	0.94	1
III	16.06	16.81	16.28	2.02	1	2.02	0.93	1
IV	11.55	12.41	11.79	1.79	1.83	1.85	0.91	1
V	13.44	14.05	13.56	1.48	1.52	1.49	0.88	1
VI	13.66	14.20	13.70	1.41	1.5	1.41	0.88	1
VII	13.82	14.33	13.92	1.45	1.41	1.43	0.87	1

In conventional method, the dc-link voltage is maintained constant for all the load conditions and evaluated as 1100 V, for 230 V (phase to neutral), 50 Hz system [6]. The proposed method reduces the dc-link voltage at reduced load

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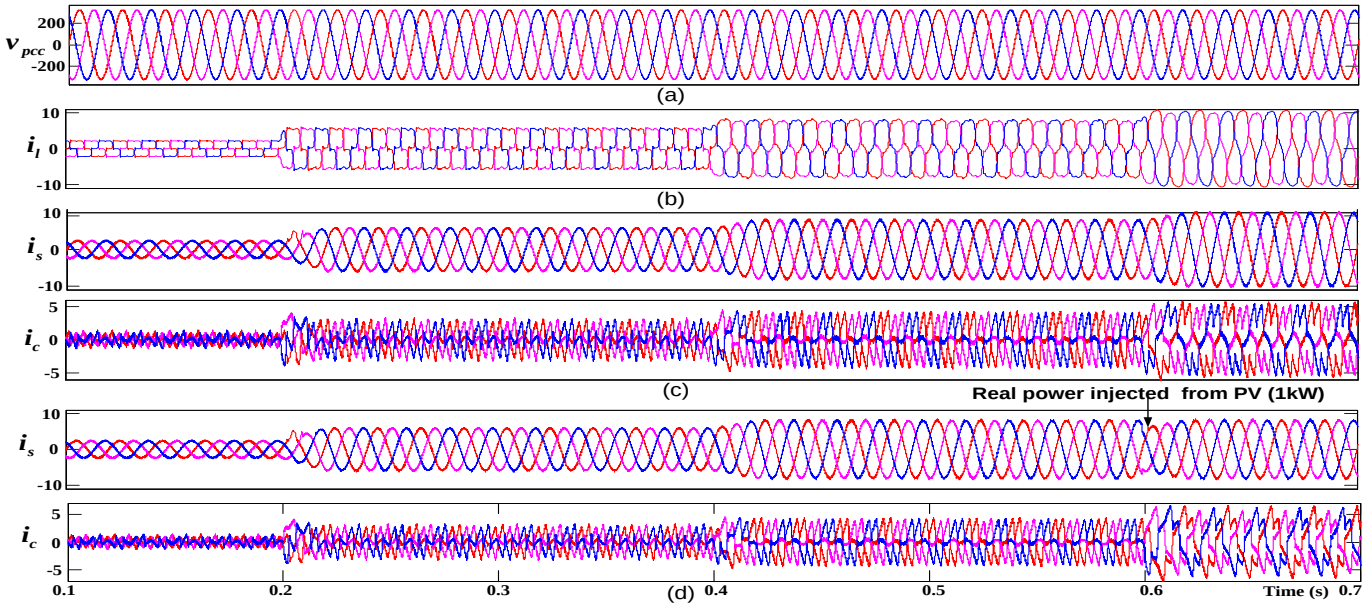

Fig. 8: Simulation waveforms for t = 0.1 s to 0.7 s: (a) PCC voltage (v_{pcc}), (b) load current (i_l), (c) and (d) source current (i_s) and compensating current (i_c) without real power injection and with real power injection, respectively.

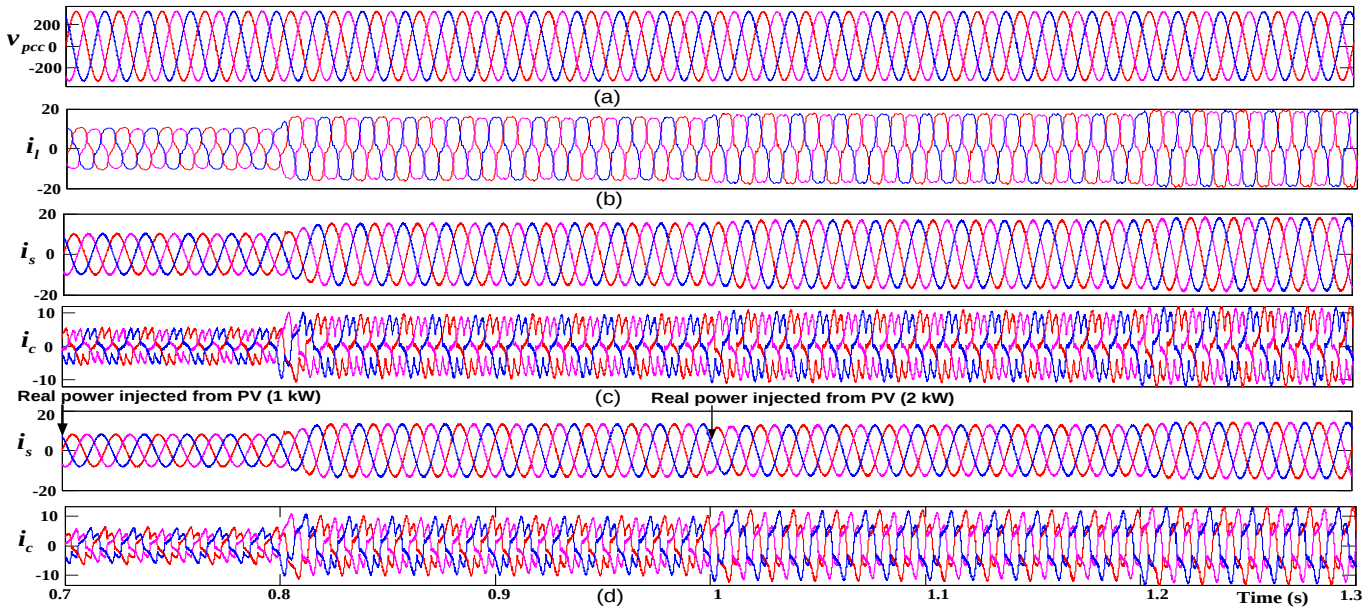

Fig. 9: Simulation waveforms for t = 0.7 s to 1.3 s: (a) PCC voltage (v_{pcc}), (b) load current (i_l), (c) and (d) source current (i_s) and compensating current (i_c) without real power injection and with real power injection, respectively.

conditions. The variation of dc-link voltage (V_{dc}) based on the ranges of reference dc-link voltage (V_{dc}^*) through the operation of RSC-MLC for various load conditions is shown in Fig. 10. I_c^* is the reference compensating current and V_{dc}^* is the estimated reference dc-link voltage to be applied for compensation. V_{dc} is the actual dc-link voltage maintained at the dc side of DSTATCOM. It can be observed that at reduced loads, lesser value of dc-link voltage is sufficient for effective compensation. This reduced dc-link voltage leads to reduction of voltage stress across switches and reduction of switching losses in VSI.

The overall switching losses (P_{sw}) are estimated from the expression of energy dissipation (E_{sw}) and is given as,

$$E_{sw} = E_{sw,n}\Big(\frac{I_{sw}}{I_{sw,n}}\Big)^{k_i}\Big(\frac{V_{sw}}{V_{sw,n}}\Big)^{k_v}(1 + TC_{sw}(T_j - T_{jn})) \tag{8}$$

where, f_{sw} is the switching frequency taken as 10 kHz, and P_{sw}=E_{sw}*f_{sw}. In (8), $I_{sw,n}$, $V_{sw,n}$, T_{jn} and energy dissipation $E_{sw,n}$ are reference values at nominal test conditions, and are obtained from the data sheet of the IGBT [20]. Here, k_i is the current dependency (=1 for IGBT), k_v is the voltage dependency (=1.2 for IGBT). TC_{sw} is the temperature coefficient of switching losses (= 0.003 for IGBT). I_{sw} and

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TABLE IV: Comparison of switching losses between conventional and proposed method without and with real power injection for different load conditions.

Case	V_{dc}^{*} (V)	V_{dc} (V)		Conventional		Proposed [P_{sw}(W) = $P_{sw,vsi}$+$P_{sw,mlc}$]						% reduction	
				P_{sw}(W) = $P_{sw,vsi}$		$P_{sw,vsi}$	$P_{sw,mlc}$	P_{sw}	$P_{sw,vsi}$	$P_{sw,mlc}$	P_{sw}		
		conven-tional	pro-posed	case-A	case-B	case-A			case-B			case-A	case-B
I	Less than 700	1100	700	7.62	-	4.44	0.024	4.464	-	-	-	41.27	-
II	700 to 766	1100	766	37.2	-	24.06	0.024	24.084	-	-	-	35.26	-
III	766 to 833	1100	833	80.58	-	57.72	0.024	57.744	-	-	-	28.34	-
IV	833 to 900	1100	900	125.64	139.05	98.76	0.024	98.784	109.26	2.352	111.612	21.37	19.73
V	900 to 966	1100	966	211.68	219.9	181.2	0.024	181.224	188.16	2.352	190.512	14.39	13.36
VI	966 to 1033	1100	1033	239.58	266.4	222.18	0.024	222.204	247.02	4.24	251.26	7.25	5.68
VII	More than 1033	1100	1100	269.04	292.26	269.04	0.024	269.064	292.26	4.24	296.5	0	-1.45[@]

case-A: without real power injection, case-B: with real power injection (1 kW in case-IV, V; 2 kW in case-VI, VII), [@]-ve sign: increase in loss due to RSC-MLC at rated load.

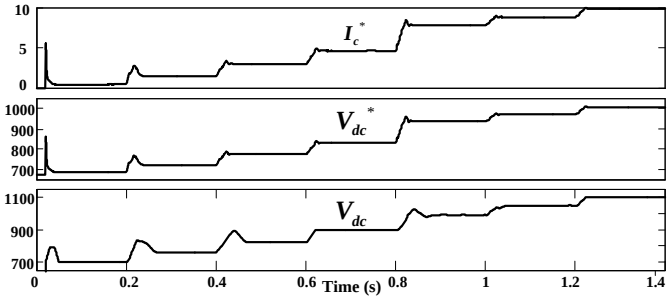

Fig. 10: Variation of dc-link voltage with operation of the proposed RSC-MLC for different loads.

V_{sw} are the current flowing through switches and blocking voltage of switches respectively. The % reduction in switching losses using proposed method, when compared to conventional method for different load conditions are tabulated in Table IV. In this table, P_{sw} denotes the overall switching loss. In case of conventional method, the switching losses take place due to the switches in VSI (S_1 to S_6), $i.e.$, P_{sw}=$P_{sw,vsi}$. The proposed method utilizes RSC-MLC having four switches (sw_1 to sw_4) to provide dc-link voltage variation, and the switching losses due to these switches $P_{sw,mlc}$ is also included in the overall loss, i.e. P_{sw}=$P_{sw,vsi}$+$P_{sw,mlc}$. The switching loss is evaluated for both the cases in Table IV, where Case-A denotes the quantities when no real power is injected from PV and Case-B denotes the quantities when there is injection of real power from PV. In case of real power injection, the switch current through RSC-MLC increased by a small amount, which leads to slight increase in RSC-MLC switching losses, but still the overall switching loss in proposed method is less for reduced load conditions.

The reduction in losses of VSI due to reduced dc-link voltage is much more compared to the losses in RSC-MLC switches. Hence, the overall switching losses is less with the proposed method compared to conventional method. The reduced switching losses makes the proposed method more efficient when compared to conventional method. In terms of design complexity, although the proposed method uses RSC-MLC, but the control algorithm is simple and effective. Considering the cost involved, the initial cost is more due to inclusion of RSC-MLC, but in the long term, it will lead to savings because the life-time of switches will increase due to reduction of the voltage stress across switches and switching losses. Therefore, the switches need not be replaced for longer durations. Also, this method utilizes PV panels as source, which encourages the use of renewable resources in the power system, making it environment friendly.

IV. Experimental Studies

The performance of the proposed variable dc-link voltage regulation method is verified with experimental prototype setup for supply voltage of 60 V (phase to neutral). The specifications of the experimental setup are, Load-1: diode bridge RL load with 20 Ω, 150 mH, Load-2: linear unbalanced load of 14 Ω, 68 mH in a-phase, 14 Ω, 25 mH in b-phase, and 14 Ω, 68 mH in c-phase. Interfacing inductance is 7.5 mH, hysteresis band h is 0.2 A, dc side capacitors (C_{dc} and C_n) value are 1.38 μF and 144 μF, respectively.

The experimental setup consists of IGBT switches based 3-leg voltage source inverter DSTATCOM with neutral capacitor. The required feedback signals such as PCC voltages, load currents, compensating currents and dc-link voltages are measured by using Hall-effect voltage and current transducers. The control algorithm is implemented in dSPACE MicroLabBox DS-1202. It acquires current and voltage signals, as well as processes to generate reference compensating currents, reference dc-link voltage and switching signals to IGBTs. The switching command signals are taken out from the master I/O pins of DS-1202 and given to inverter switches with proper isolation.

A. Compensation Performance of the DSTATCOM

The experimental waveforms of PCC voltage (v_{pcc}), source current (i_s), load current (i_l) and compensating current (i_c) during load variation for phase-a, b and c are shown in Fig. 11. It is observed from Fig. 11(a)-(c), that even with load variations, the source current (i_{sa}, i_{sb}, i_{sc}) becomes balanced, sinusoidal and in-phase with corresponding phase voltage (v_{sa}, v_{sb}, v_{sc}), respectively.

In the proposed method the dc-link voltage is varied corresponding to load variation as shown in Fig. 12. It is observed

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that, the dc-link voltage required for load-1 is 104 V and for load-2 is 134 V, calculated using the proposed method. But, in conventional method the dc-link voltage is maintained at rated value for any load condition ($i.e.$, 272 V for the 60 V supply system). For better understanding the compensation performance, the waveforms during load-1 and load-2 are zoomed and shown in Fig. 12(b) and 12(c), respectively.

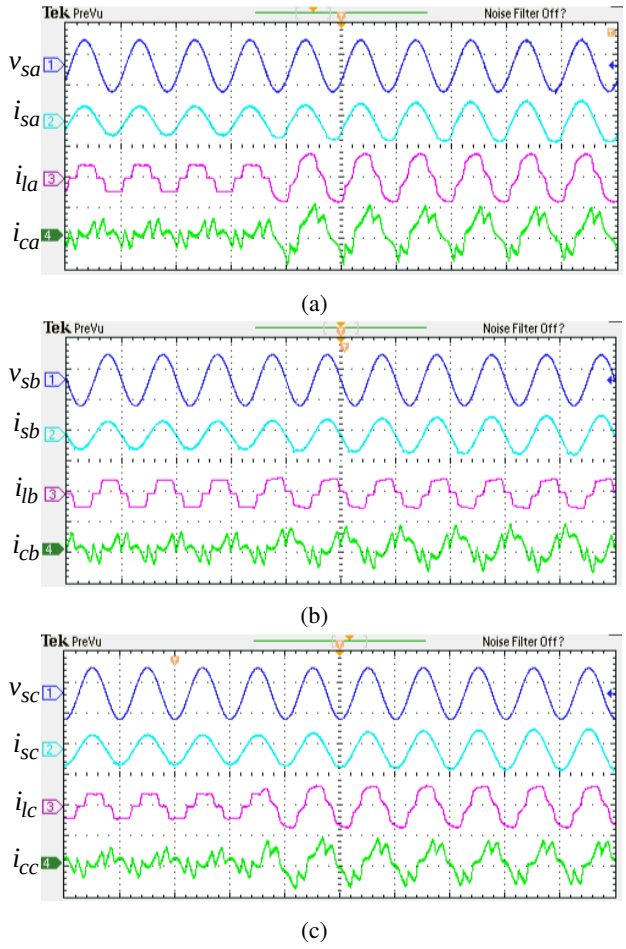

Fig. 11: (a) phase-a, (b) phase-b and (c) phase-c waveforms for load variation (Load-1 to Load-2).

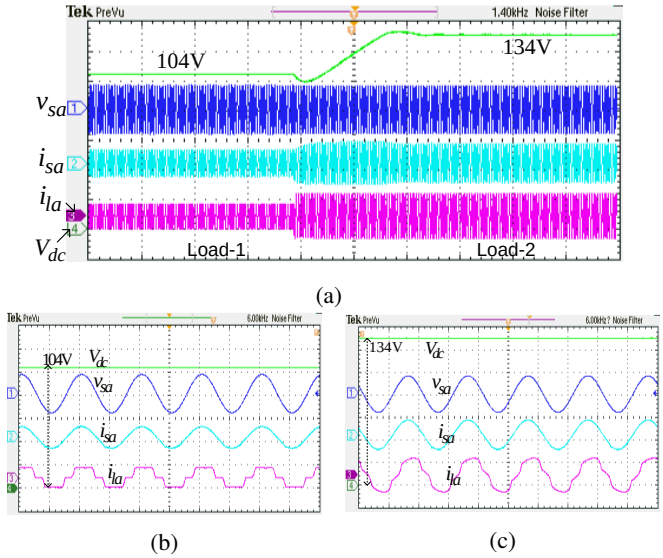

Fig. 12: (a) dc-link voltage variation for load change, (b) and (c) are zoomed waveforms of 12(a) for load-1 and load-2 respectively.

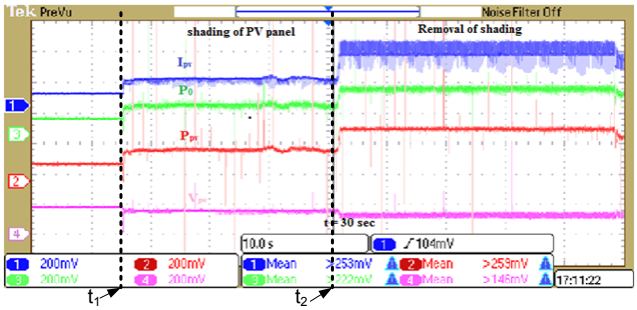

Fig. 13: MPP tracking waveforms with HGBC.

B. PV Power Injection along with Reactive Power Compensation

The MPP tracking waveforms with high gain boost converter are shown in Fig. 13. It is observed that, the MPP tracking starts at t_1, and algorithm works for change of irradiation at t_2. The variable irradiation situation is obtained by shading the panels. The PV system is integrated in dc side of the DSTATCOM for real power injection and to maintain the dc-link voltage. Fig. 14(a), shows the waveforms before and after PV power injection along with compensation. It is observed that for the fixed load current, the source current is decreased when PV system is injecting part of real power demanded by load. The three-phase source currents and phase-a load current before and after PV power injection along with compensation are shown in Fig. 14(b). It is observed that, the source currents are reduced when real power injected. The average real power drawn from source in phase-a, b, c are shown in Fig. 14(c). It is observed that, at stage-1, because of PV power injection, the real power drawn from source is decreased from 0.049 kW to 0.036 kW. At stage-2, PV power injection increases because of more irradiation, therefore real power from source still reduced to 0.024 kW.

The harmonic spectrum and phasor diagram for load-2, before and after compensation are shown in Fig. 15. Fig. 15(a) represents, the harmonics spectrum of three-phase source currents before compensation. It is observed that, the phase-a, b, c source current have THD of 11.6%, 20.8% and 11.6%, respectively. After compensation, the three-phase source currents THDs are reduced to 2.9%, 2.6% and 3.2%, respectively are shown in Fig. 15(b). Fig. 15(c) represents, phasor diagram before compensation with phase-a, b, c currents 2.2 A, 1.3 A, 2.1 A lags the corresponding voltages by 26°, 22°, 22°, respectively. After compensation, the source currents are in-phase with voltages as shown in Fig. 15(d).

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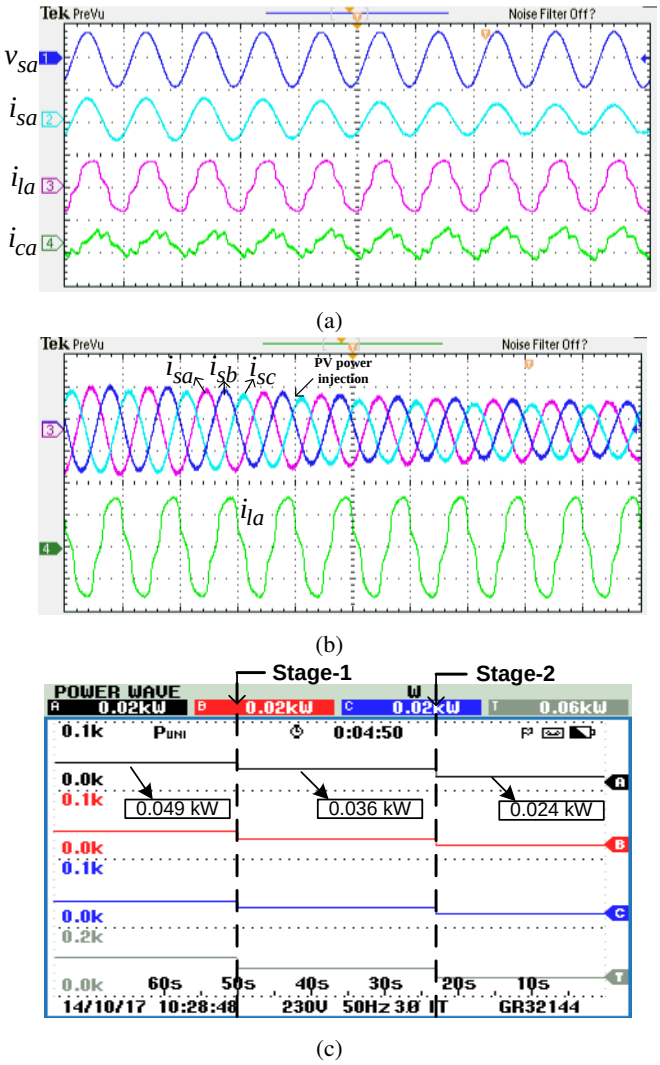

Fig. 14: (a) and (b) Before and after PV connected along with Compensation, and (c) Average real power drawn from source in a, b and c phases.

V. Conclusion

A new method is proposed to regulate the dc-link voltage using RSC-MLC without affecting the performance of DSTATCOM. It also uses renewable energy resources for obtaining dc voltage source such as PV panels, Fuel cells. Using PV panels effectively enables it to deliver real power as well as compensation to the load during day time and work purely as DSTATCOM for power quality improvement at night. It can be observed from simulation and experimental results that compensation for reactive power and harmonics has been achieved effectively. The source current is balanced, sinusoidal, distortion-free and with improved power factor. The %THD has reduced significantly after compensation. Also, due to reduced dc-link voltage at lesser loads, voltage stress across the switches has reduced and switching losses are minimized to a great extent, increasing the life-time and efficiency of DSTATCOM. Hence, it can be a good alternative for power quality improvement and real power support to the load.

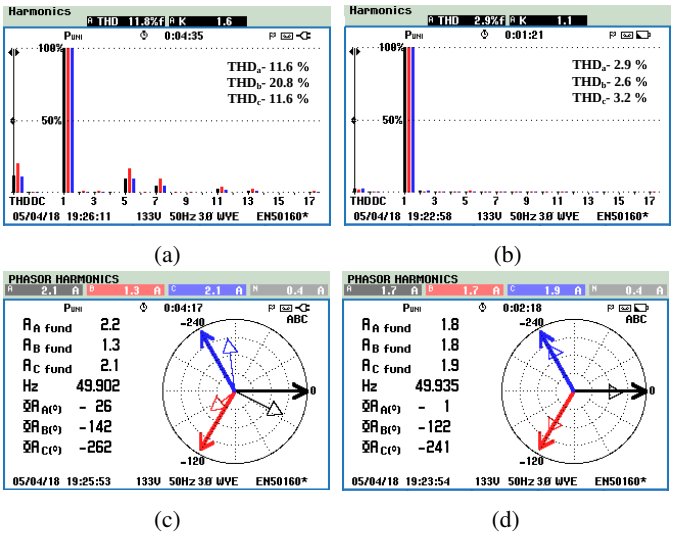

Fig. 15: (a) and (b) Harmonic spectrum of source current before and after compensation for load-2, (c) and (d) phasor diagrams before and after compensation for load-2.

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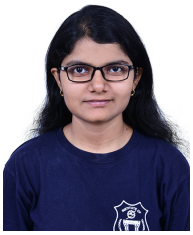

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